CLAIMS

What is claimed is:

1. A method for reducing capacitance between interconnect lines, the method comprising:

providing a substrate having a plurality of semiconductor elements and one dielectric layer for isolating the semiconductor elements formed thereon;

forming a metal layer over said substrate;

forming a pad oxide layer over said metal layer;

pattering and etching said pad oxide layer and metal layer to constitute said interconnect lines over said substrate;

forming an inter-metal dielectric layer over said substrate having said interconnect lines formed thereon, wherein at least an air gap is formed in a spacing between the adjacent interconnect lines; and

planarizing said inter-metal dielectric layer.

2. The method according to claim 1, wherein said metal layer is formed from materials selected from the group consisting of Al, Cu, Ta, W, Si, Au, Pb and Sn.

3. The method according to claim 1, wherein the thickness of said pad oxide layer is between about 2000 angstronm and about 5000 angstronm.

4. The method according to claim 1, wherein said pad oxide layer comprises SiO_2, deposited by atmospheric pressure CVD method.

5. The method according to claim 1, wherein said pad oxide layer comprises SiO_2, deposited by plasma enhanced CVD method.

6. The method according to claim 1, wherein said inter-metal dielectric layer comprises a SiO_2 layer, deposited by plasma enhanced CVD method, utilizing TEOS/O3 as reaction gas.

7. The method according to claim 1, wherein said inter-metal dielectric layer comprises a BPSG layer, deposited by atmospheric pressure CVD method, utilizing TEOS/O_3, TMPO and TEB as reaction gas, at temperature lower than 550℃.

8. The method according to claim 1, wherein said inter-metal dielectric layer comprises a BPSG layer, deposited by plasma enhanced CVD method, utilizing TEOS, O_3/O_2, TMP and TMB as reaction gas, at temperature between about 400℃ and 500℃.

9. An interconnect structure, the structure comprising:

a substrate having a plurality of semiconductor elements and one dielectric layer for isolating the semiconductor elements formed thereon;

a plurality of adjacent interconnect lines having spacings therebetween with different aspect ratios with at least an air gap formed therein formed over said substrate, each of which comprising a lower metal line and a top pad oxide layer, said air gap is positioned below said pad oxide layer and the level of the top end of said air gap is beyond the upper ends of said adjacent metal lines, and the level of the lower

end of said air gap is below the bottom ends of said adjacent metal lines; and

an inter-metal dielectric layer formed over said substrate having said adjacent interconnect lines formed thereon.